II Year-I Semester		**T**	**P**	**C**
		0	**3**	**2**
DIGITAL LOGIC DESIGN LAB (RT21056)				

Course Description and Objectives:

Acquaintance with the basic mathematical implication for computer science, applications of mathematics in computer science

Course Outcomes:

Upon completion of the course,the student will be able to achieve the following outcomes.

Cos	Course Outcomes	POs
1	Design and test behaviour of basic logic gates	4
2	Design and test behaviour of universal gates using basic logic gates	5
3	Design the circuit and test behaviour of demorgans law.	5
4	Design and test behaviour of the following combinational circuits: Adders/Subtractors, encoders/decoders, (de)multiplexers, comparators	8
5	Design and test behaviour of the basic flip-flops.	7
6	Design and test behaviour of the sequential circuits, like counters and shift registers.	5

List of Experiments:

1) Verification of Basic Logic Gates.
2) Implementing all individual gates with Universal Gates NAND & NOR.
3) Design a circuit for the given Canonical form, draw the circuit diagram and verify the De-Morgan laws.
4) Design a Combinational Logic circuit for 4x1 MUX and verify the truth table.
5) Design a Combinational Logic circuit for 1x4 De-MUX and verify the truth table.
6) Verify the ***data read*** and ***data write*** operations for the IC 74189.
7) Design a Gray code encoder and interface it to SRAM IC 74189 for write operation display on 7-segment.
8) Design a Gray code De-coder and interface it to SRAM IC 74189 for read operation display it on 7-segment.
9) Construct Half Adder and Full Adder using Half Adder and verify the truth table.
10) Verification of truth tables of the basic Flip- Flops with ***Synchronous*** and ***Asynchronous*** modes.
11) Implementation of Master Slave Flip-Flop with J-K Flip- Flop and verify the truth table for ***race around*** condition***.***
12) Design a Decade Counter and verify the truth table.
13) Design the Mod 6 counter using D-Flip -Flop.
14) Construct 4-bit ring counter with T-Flip –Flop and verify the truth table.
15) Design a 8 – bit right Shift Register using D-Flip –Flop and verify the truth table.